Fujitsu SPARC64™ VI: A State of the Art Dual-Core Processor

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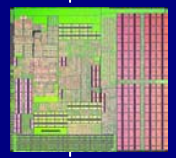
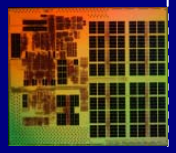
SPARC64™/GS CPU Roadmap



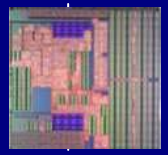
SPARC64™ V
1.35GHz
130nm



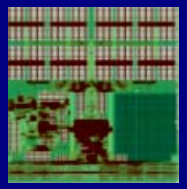
SPARC64™ V +
1.89GHz
90nm
2.16GHz
90nm

SPARC64™ VI
2.4GHz
90nm
2-core x 2-thread

SPARC64™ VII
~2.7GHz
65nm
4-core x 2-thread



GS21 model600
130nm



GS21 model900
90nm

Mainframe RAS → **Multi-Threaded Processor**

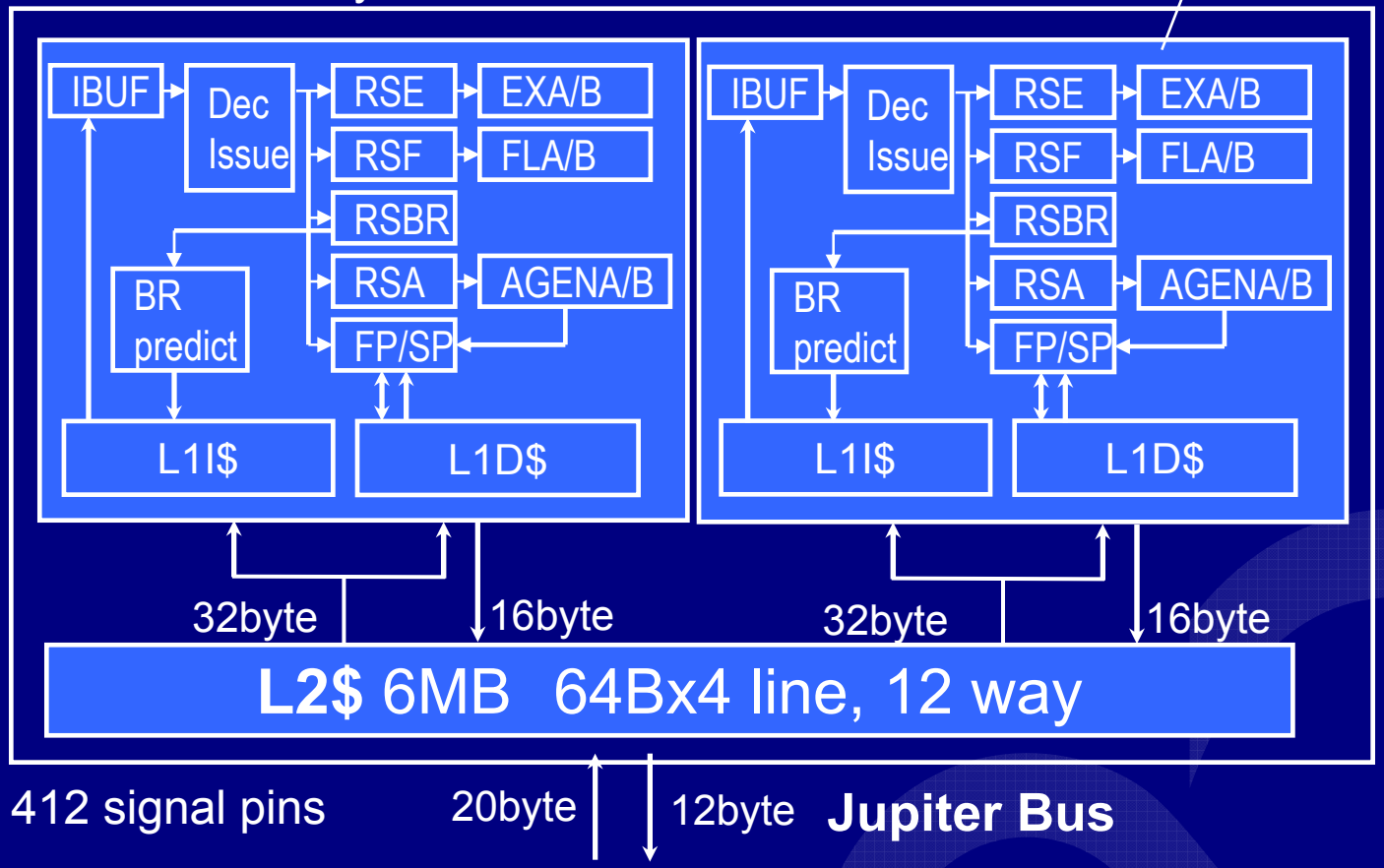
2003 2004 2005 2006 2007 2008

- This road map is a previous notice and might change.

SPARC64™ VI

SPARC64™ VI Chip

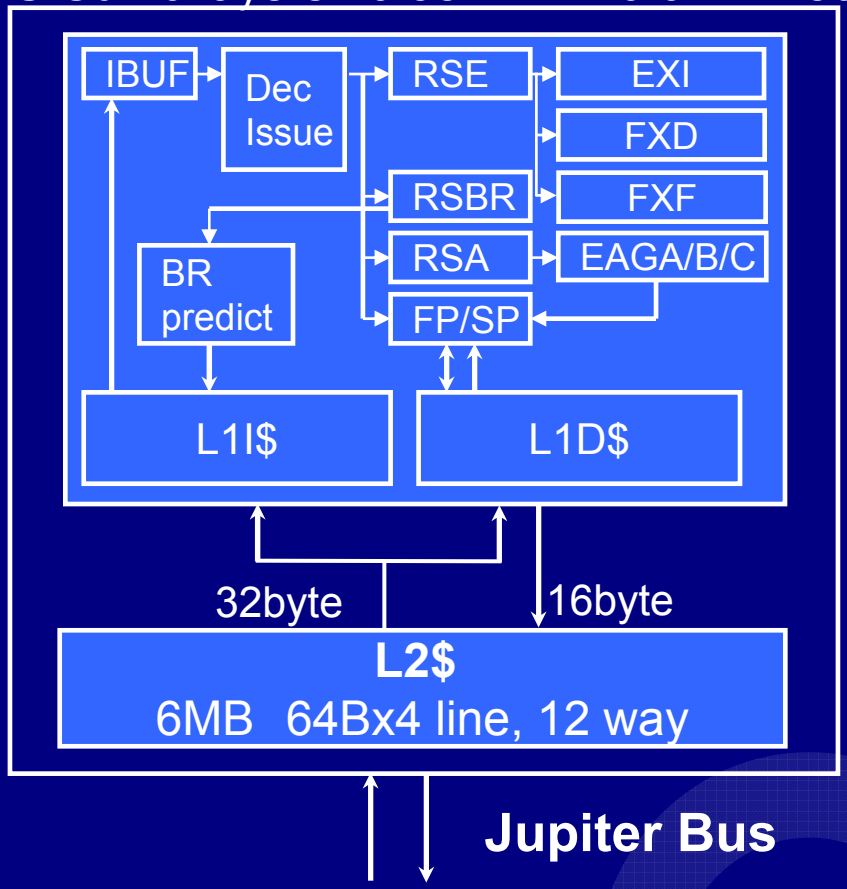
90nm CMOS Cu 10 layers 20.38mm x 20.67mm 540M transistors



- Multi-Threaded Processor 2core x 2threads
- 2.4GHz
- 120 W(max.)

The latest Mainframe CPU Chip

90nm CMOS Cu 10 layers 20.38mm x 20.67mm 500M transistors



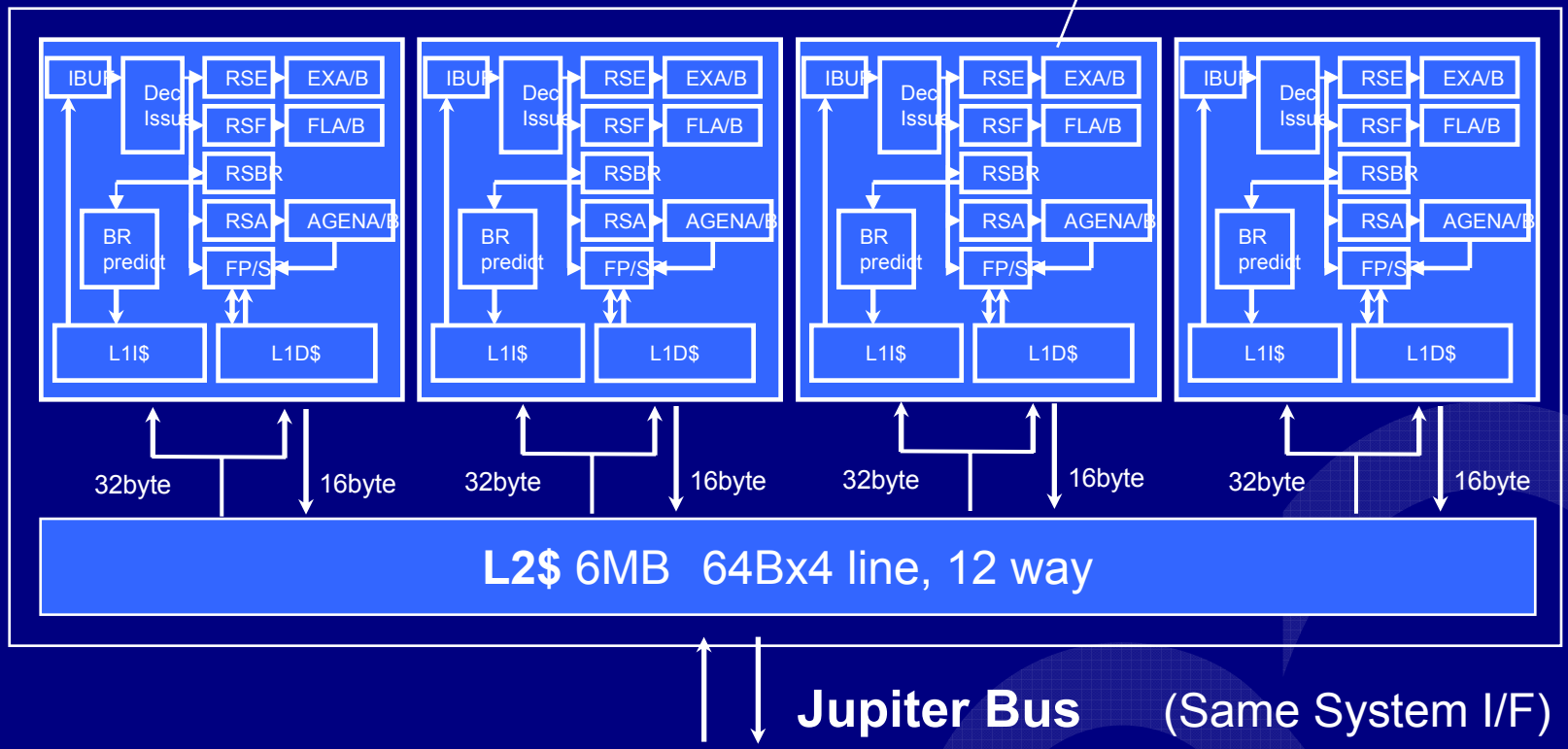
Enhancements
- L2$ 6MB
- Jupiter Bus

SPARC64™ VI

SPARC64™ VII Chip

65nm CMOS 21.8mm x 21.3mm (TBD)

Enhanced
SPARC64™ VI core



Jupiter Bus (Same System I/F)

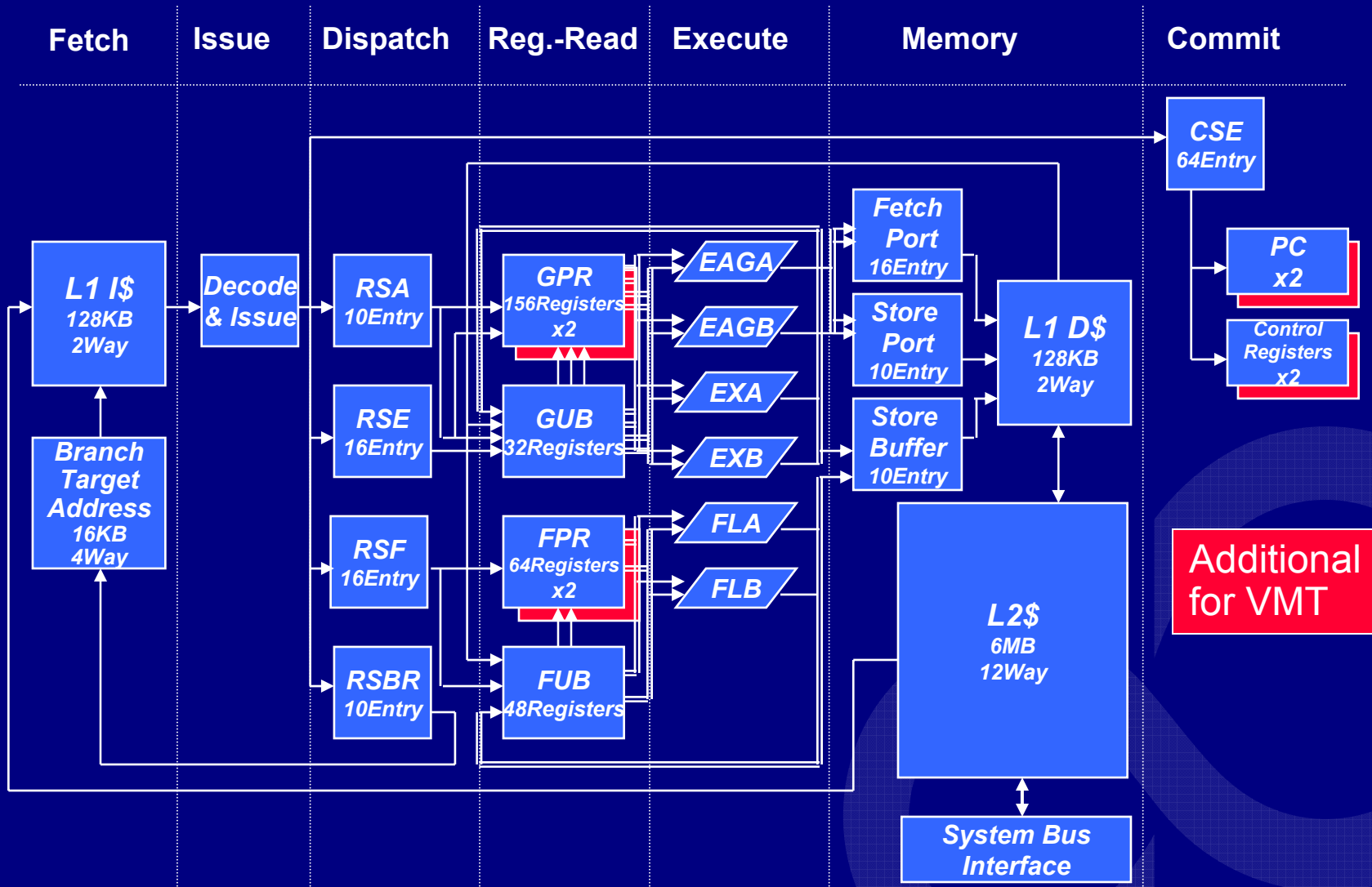
Enhancements

Multithreaded processor 4core x 2threads

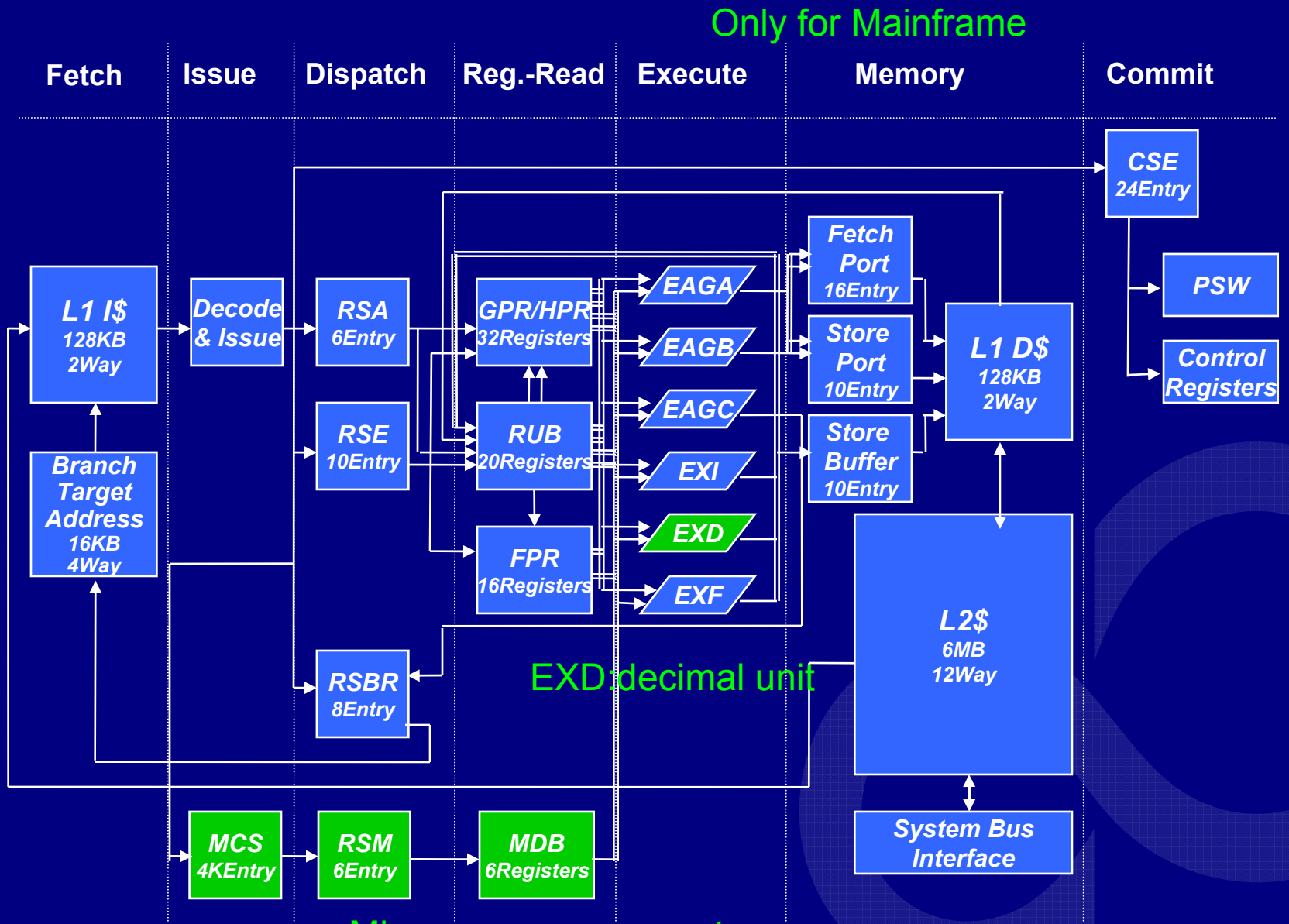
~2.7GHz

SPARC64™ VI

Pipeline structure of SPARC64™ VI

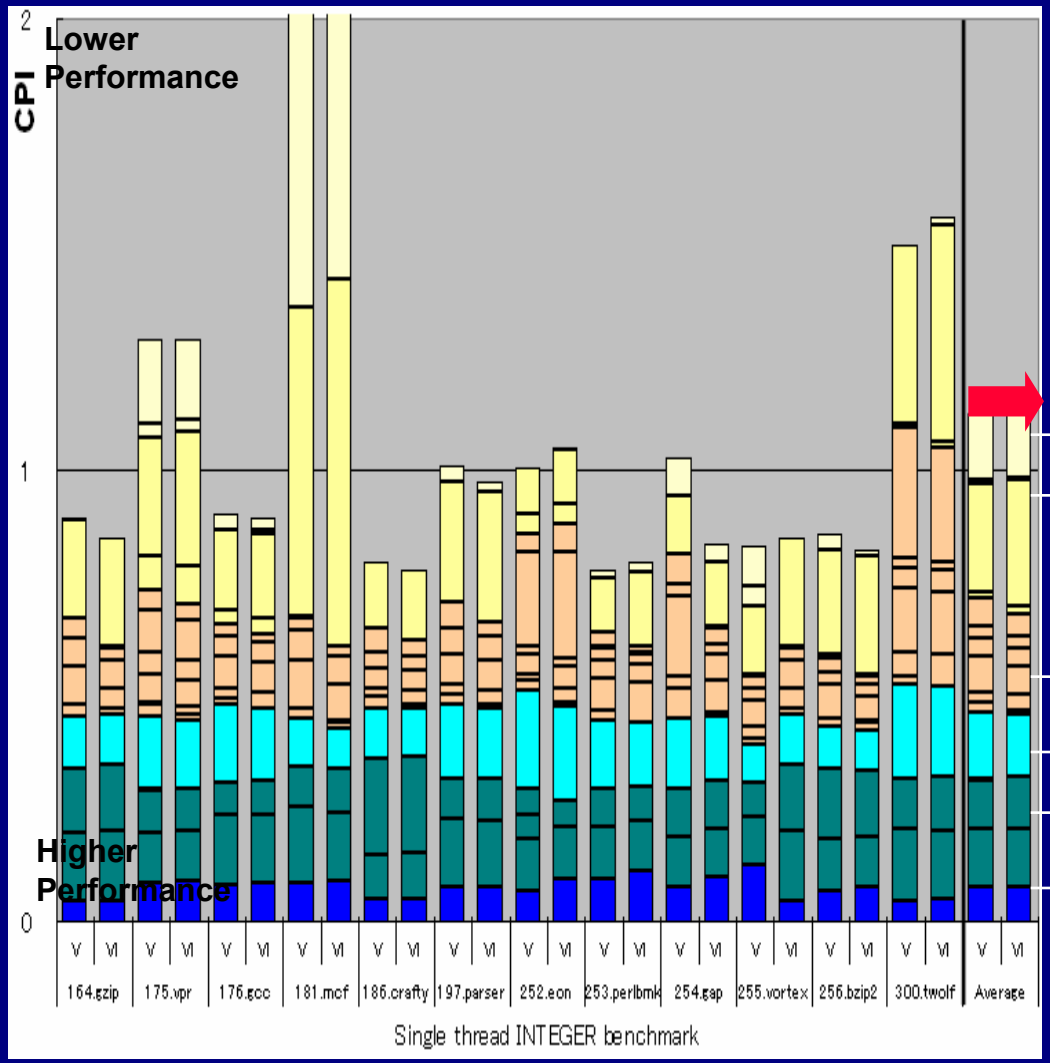


Microarchitecture of Mainframe CPU



SPARC64™ VI

INT performance relative to SPARC64™ V

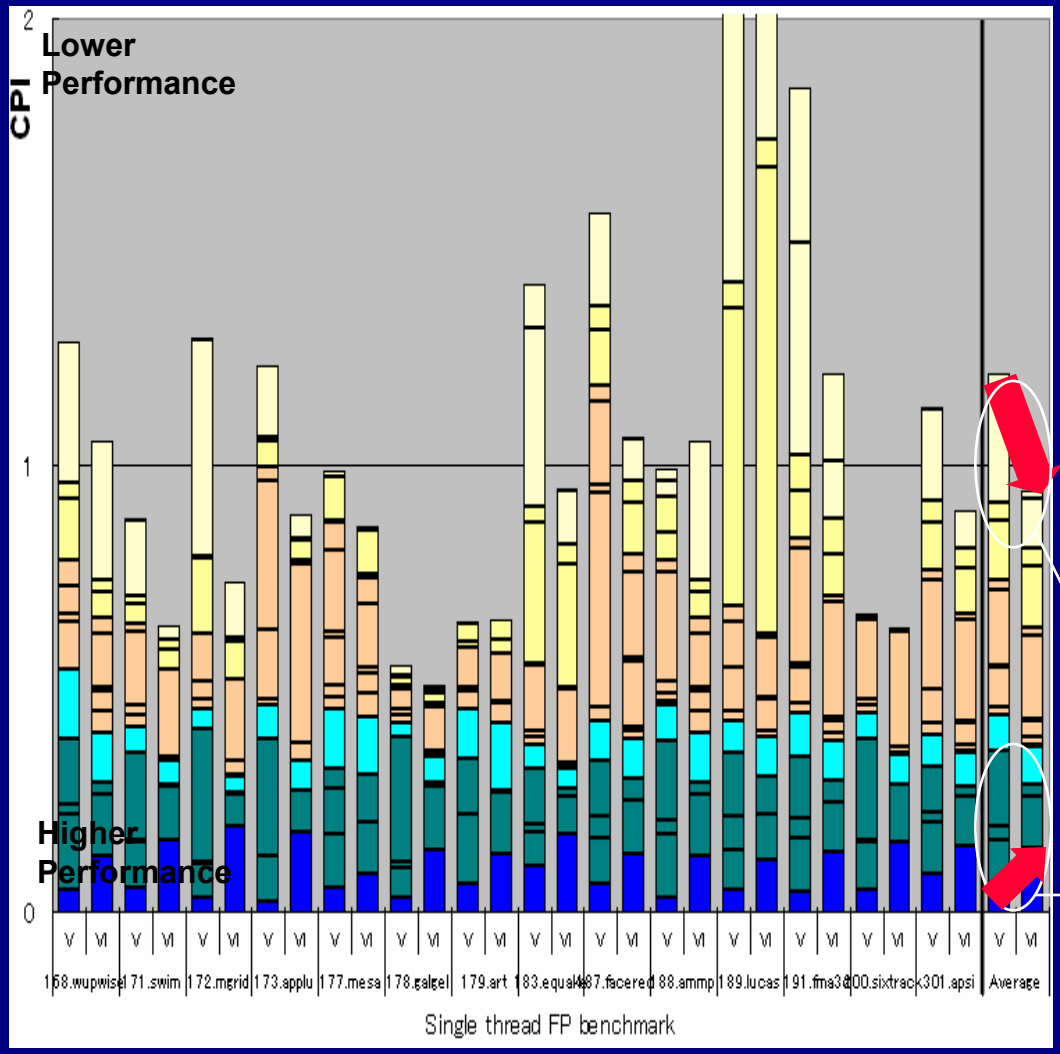


- Same INT performance per core
- Twice the performance per socket

Comparison based on SPARC64V optimized binaries

SPARC64™ VI

FP performance relative to SPARC64™ V



- +25% FP performance per core
  - High BW system bus
  - 4write ports in the FP register file
- 2.5 times FP performance per socket

Reduced memory access overhead

Increased 4 Commit ratio

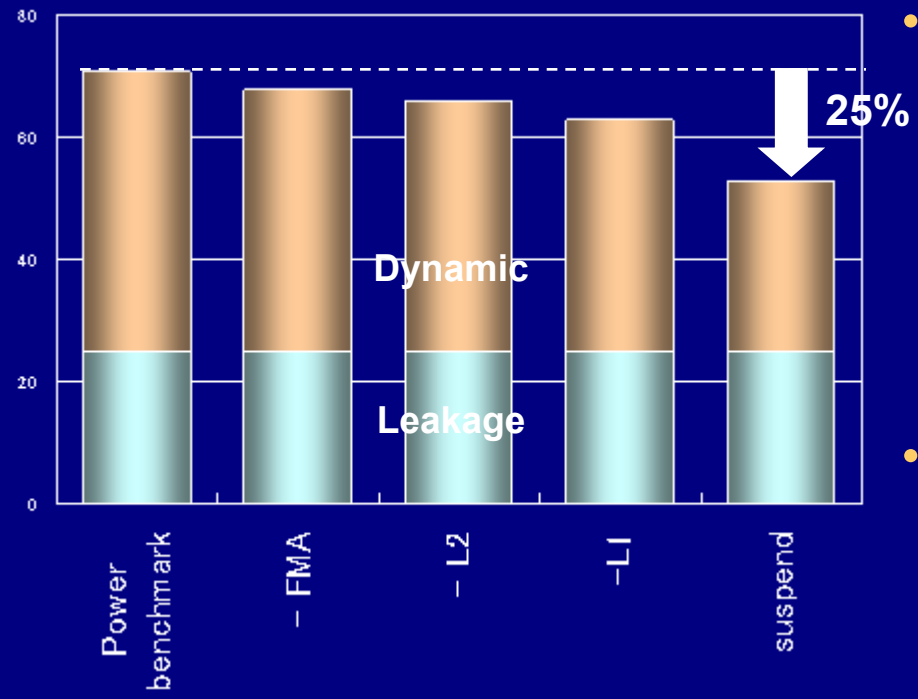
Comparison based on SPARC64V optimized binaries

SPARC64™ VI

SPARC64VI Power Consumption

- Max: 120W
- Typical: 80W = 55W(dynamic) + 25W(leakage) [Estimated]

- Power consumption [Measured]



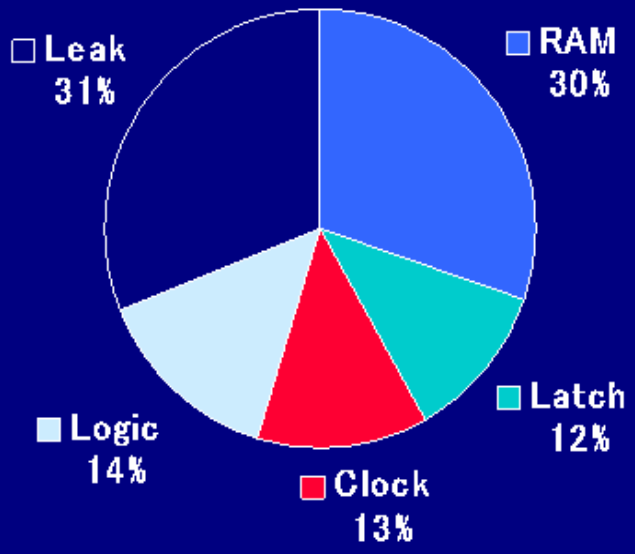
- Power benchmark
  - Internal benchmark forces SPARC64V to consume max PWR
  - Access FMA/L1$/L2$
- Suspend state (per thread)
  - No instruction is executed
  - An idle thread enters a suspended state.

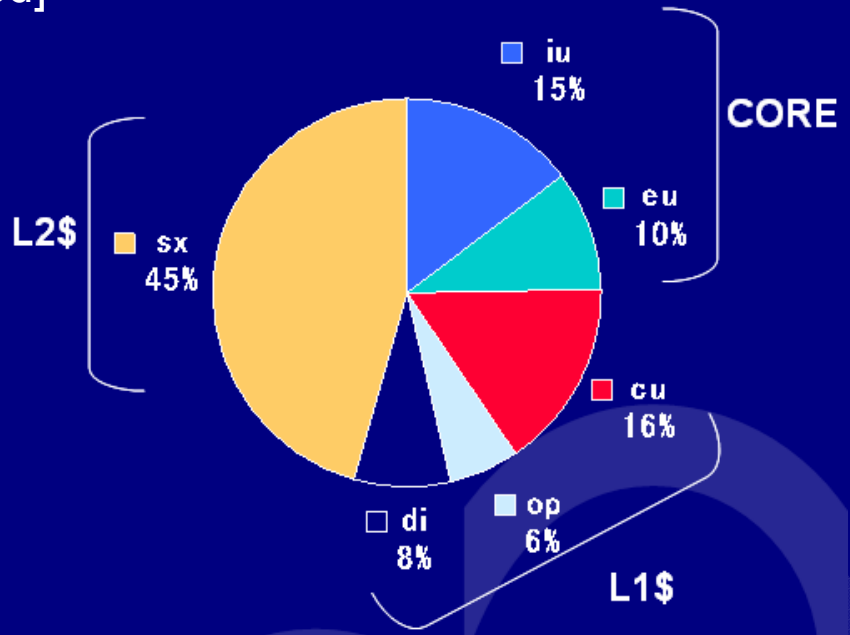
SPARC64VI Power Saving techniques

- Dynamic power saving
  - H-Tree clock distribution
  - Latch
    - Pulsed latch
    - Clock gating (IH input)
      30,000 out of 55,000 latches have this feature.
    - No system clock to slave latch to reduce load whenever applicable
  - RAM control
    - Enable word-driver, column decoder, Sense Amp on demand
- Leakage power saving
  - Multi-Vth
    - Normal Vth = 55%, High Vth = 45% of total area
  - Thicker Capacitors

SPARC64VI Power Distribution

Typical power distribution [Estimated]

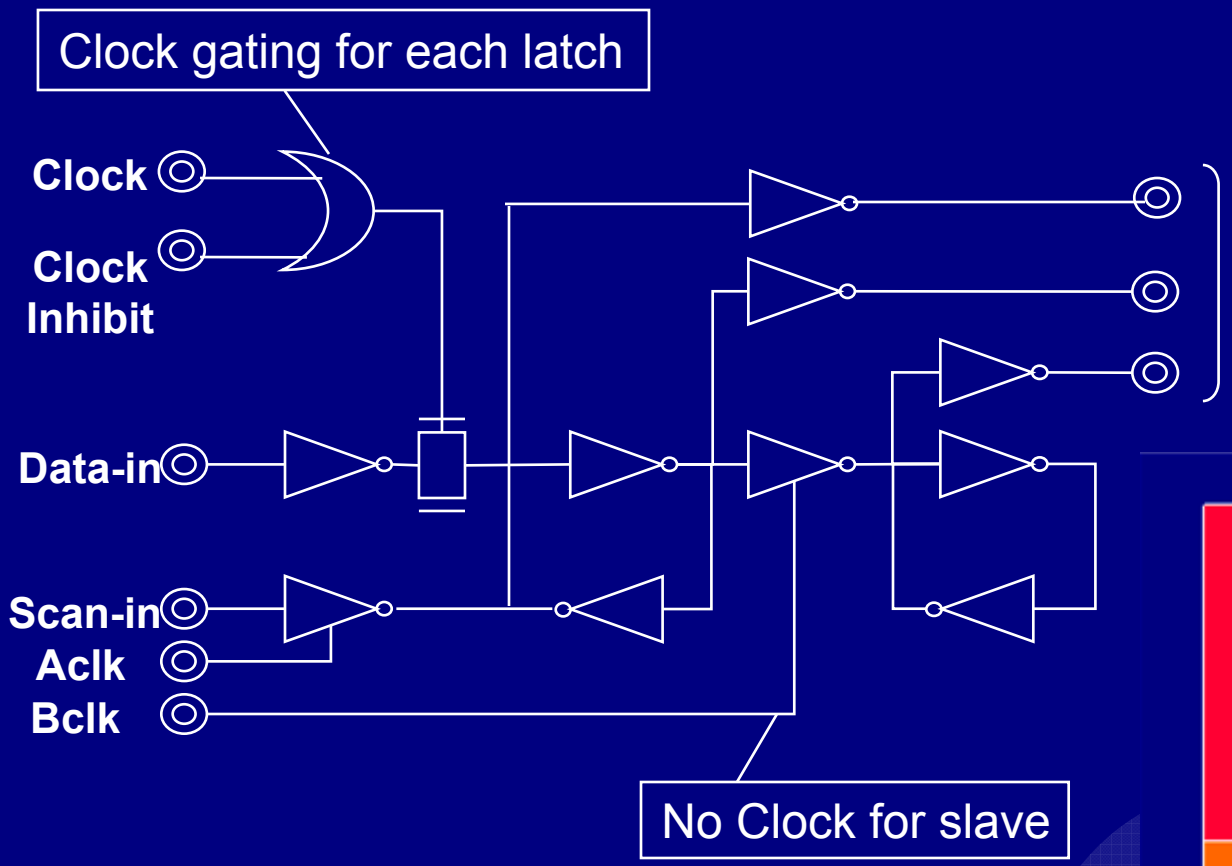


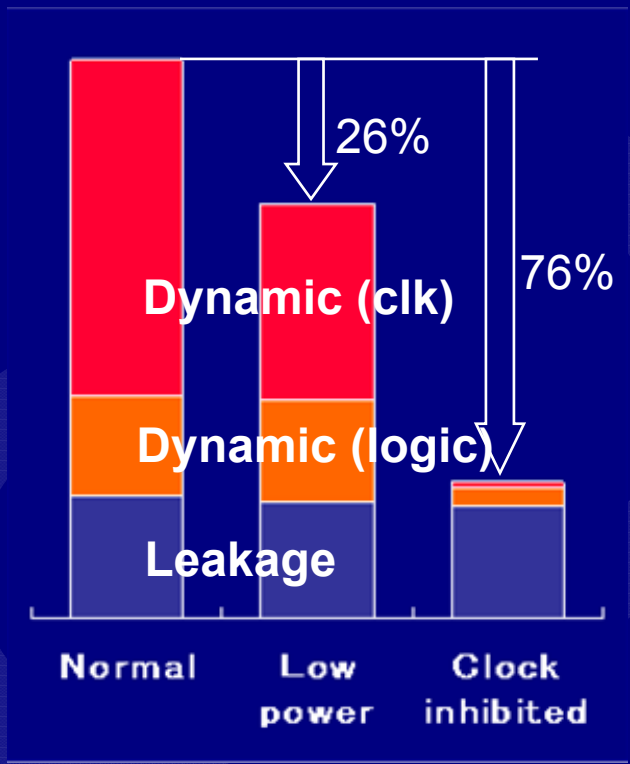


➔ Areas of focus for power reduction

- Clock/Latch
- RAM
- Leak

Low power Latch example



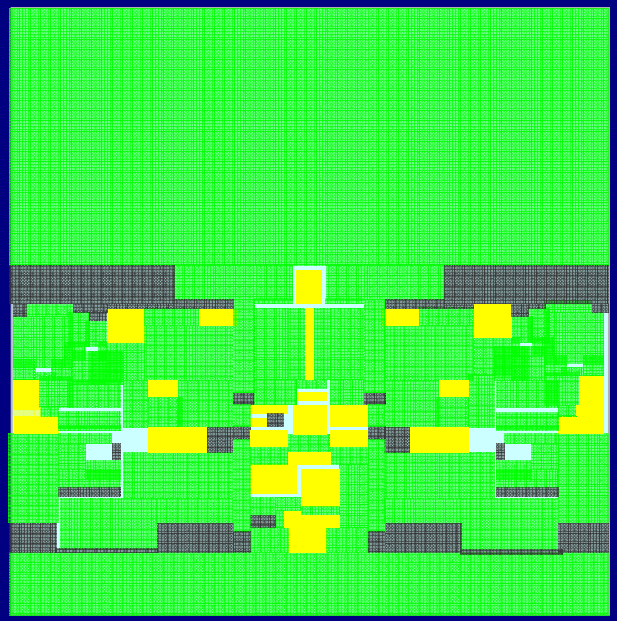


26% power reduction by low power latch

76% power reduction by clock inhibit

Reliability, Availability, Serviceability

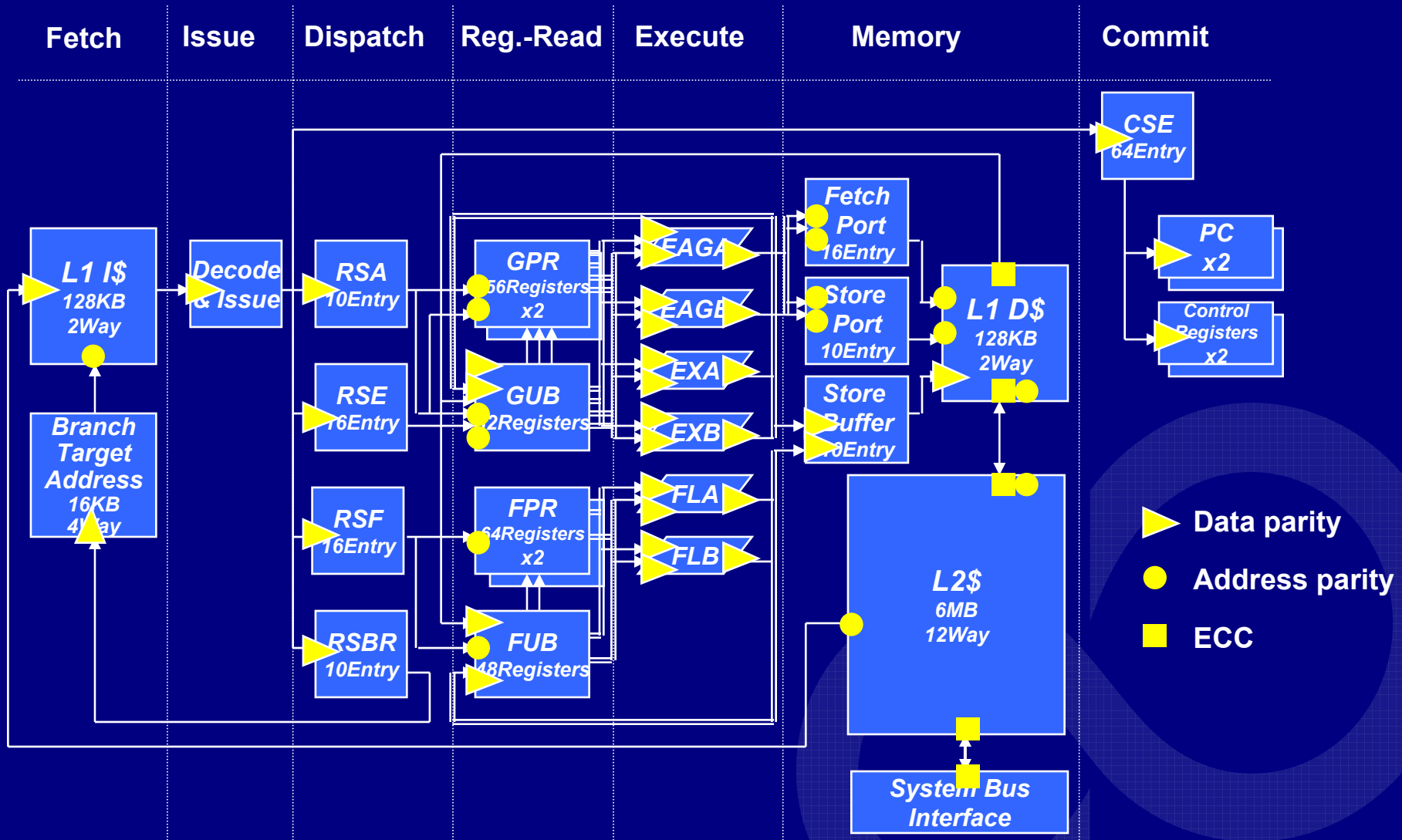
		SPARC64™ VI
Cache protection	Tag	ECC (L1$: Duplicated & Parity)
	Data	ECC
Cache dynamic degradation		Yes
ALU / Register		Parity
HW Instruction Retry		Yes
History		Yes



- Guaranteed Data Integrity
  - All RAMs are ECC protected or Duplicated
  - Most latches are parity protected

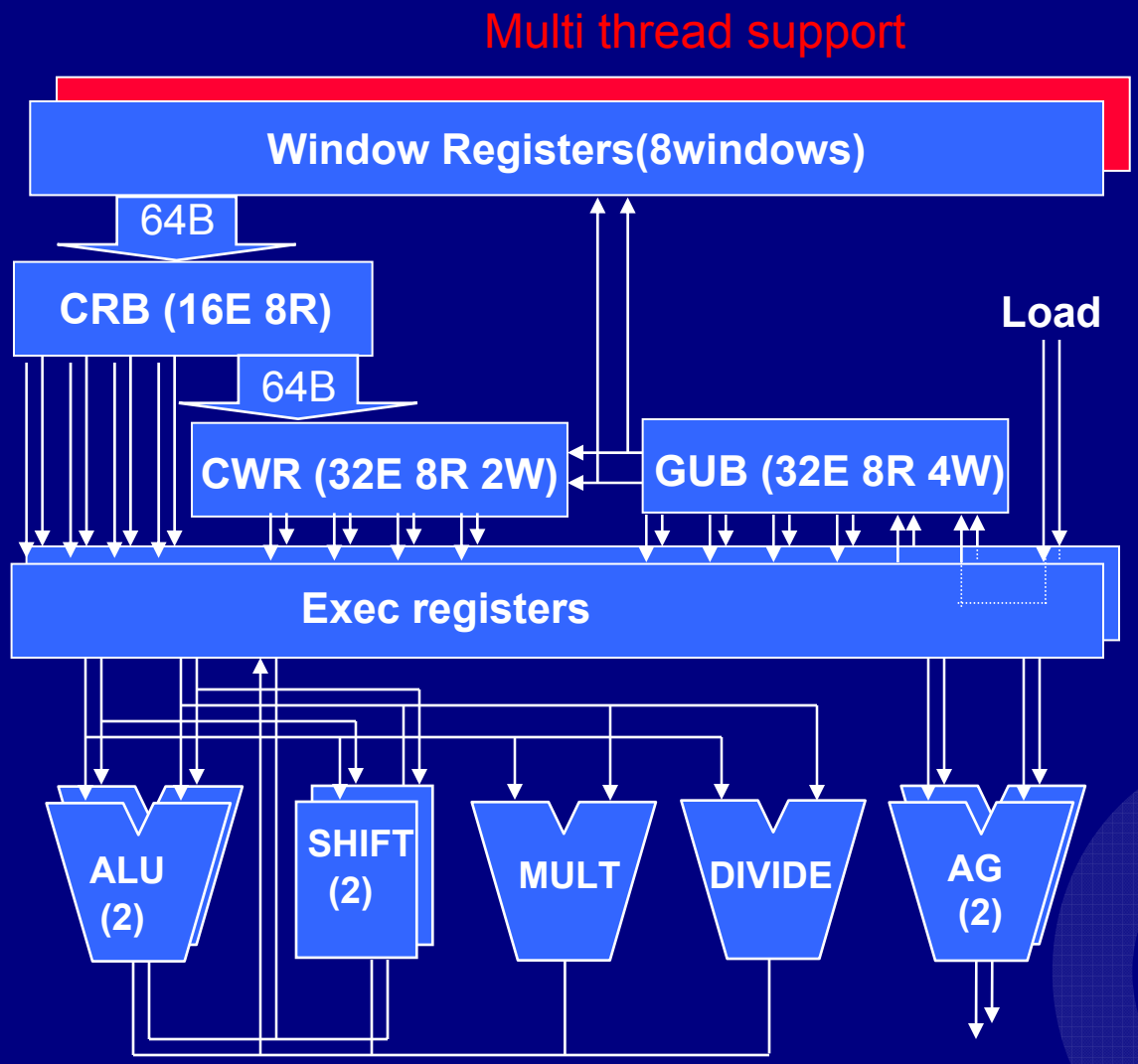
- RAS Coverage
  - Green: 1bit error Correctable
  - Yellow: 1bit error Detectable
  - Gray: 1bit error harmless

SPARC64™ VI Error Detection



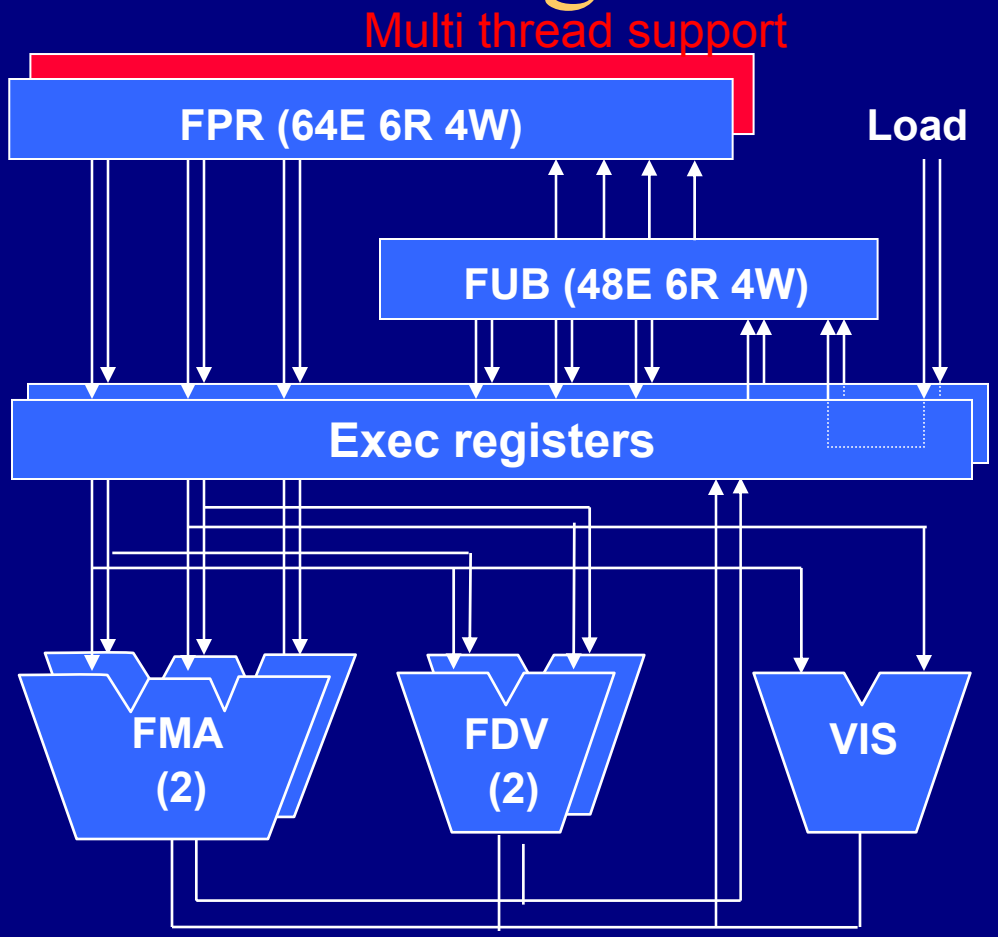
SPARC64™ VI

SPARC64 VI EX and EAG



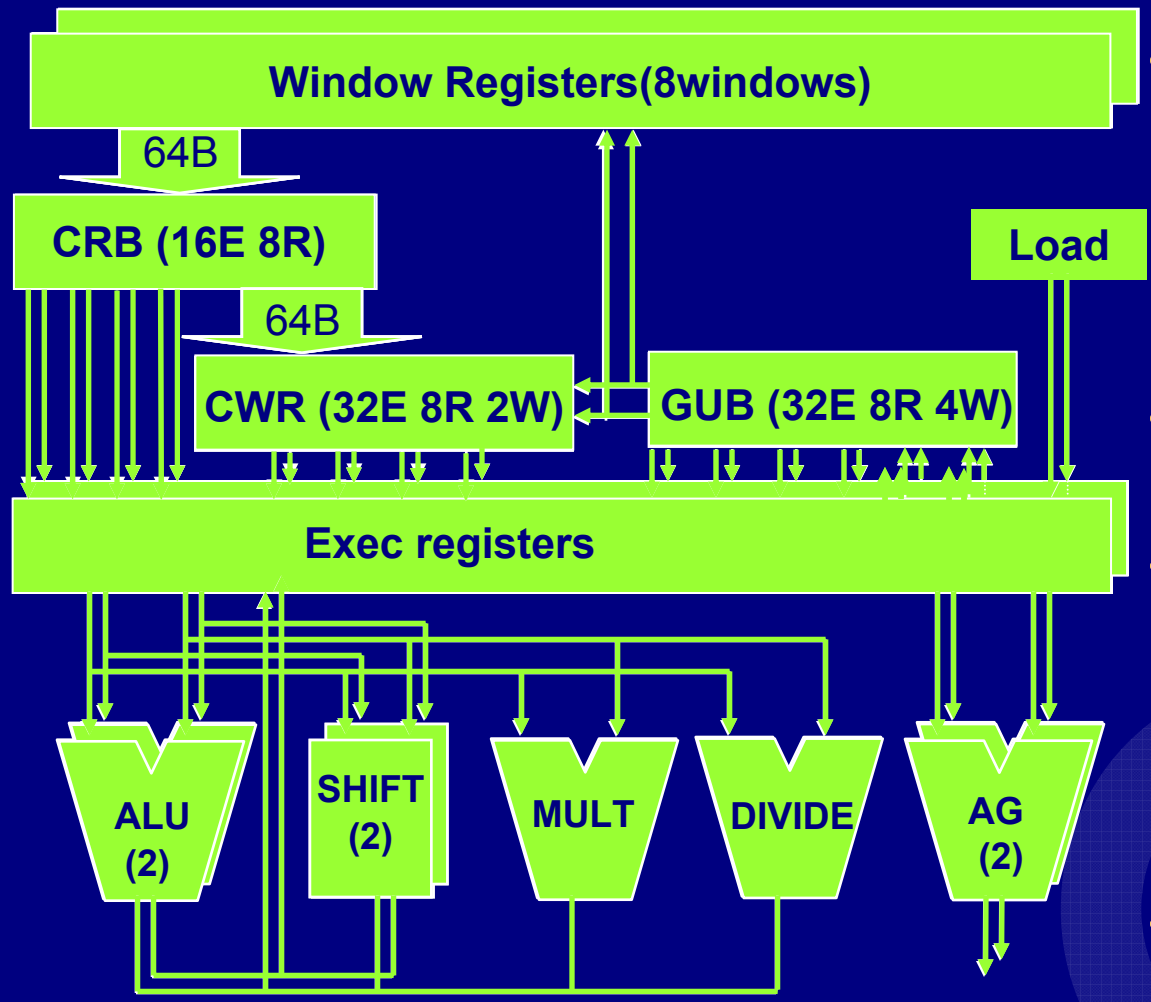
- Window Registers
- Current Window Replace Buffer (CRB)
  - Half window
  - No loss at window switch
- Current Window Register (CWR)
  - 1 window
- GPR Update Buffer (GUB)
- 4 operations in parallel
  - add,sub,and,or,shift,..
  - agen
  - Any combination

SPARC64 VI
Floating Point execution unit



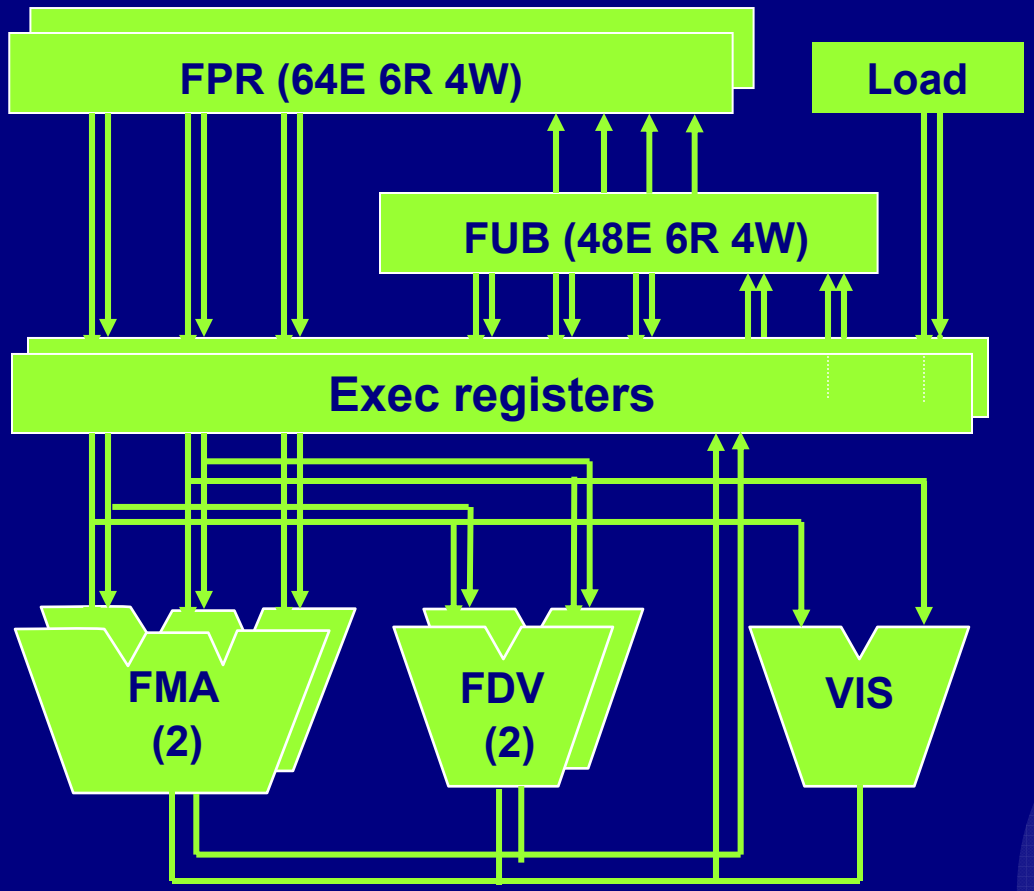
- FPR Update Buffer (FUB)
- 2 operations in parallel
  - fmul,fma,fdiv,sqrt,fadd
  - Any combination
- Fused Multiply & Add

EX and EAG -Error detect



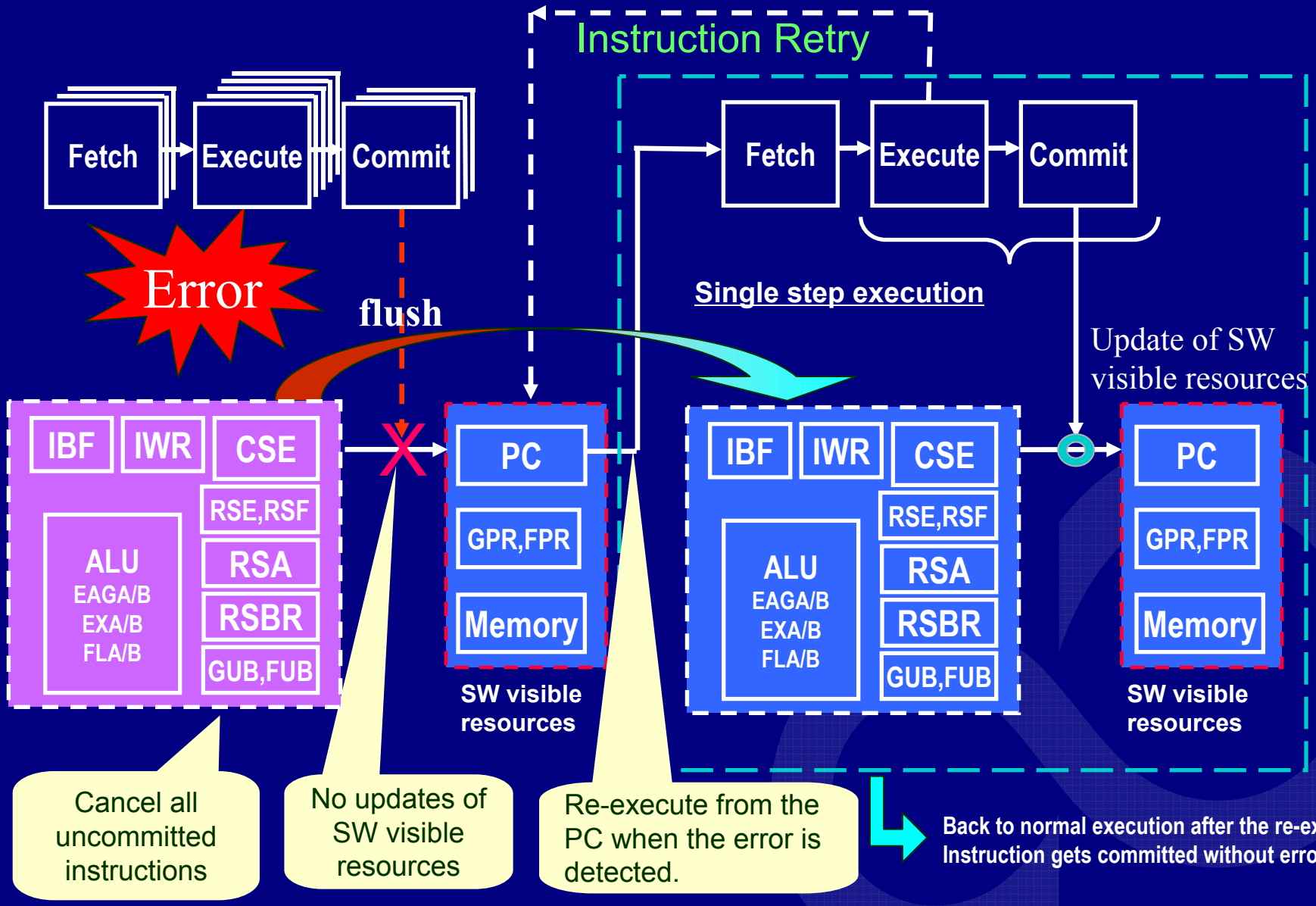
- Parity checked
  - Exec registers
- Parity protected
  - Window Registers
  - CRB, CWR
  - GUB
  - Load data
- Parity propagate
  - Every read & write bus
- Parity prediction
  - ALU
  - SHIFT
  - DIVIDE
  - AG
- Modulo-3 residue check
  - MULT

Floating Point execution unit -Error Detect



- Parity checked
  - Exec registers
- Parity protected
  - FPR
  - FUB
  - Load data
- Parity propagate
  - Every read&write buses
- Parity prediction & Modulo-3 residue check
  - FMA
  - FDV
  - VIS

Instruction Retry Mechanism



SPARC64™ VI

Accelerated soft error testing*1 of SPARC64™ V

	Static hold test error count/time (total time of 2 or 4 CPU)	Dynamic test Running test program @4CPU, 2hour3min affection/error count	Successful recovery rate
Latch	189/100800s=6.75/h*2	0/3*4	100%
RAM	3766/11100s=1221/h*3	1*5/3953	99.96%
Total	1228/h	1/3958	99.96%

*1:Utilizing a neutron beam facility in Research Center for Nuclear Physics of Osaka University.
Estimated acceleration ratio is 60M to 130M times.

*2:Stop the clock and hold the data and scan-out the latches after the test interval. This test targets 97% of the chip's latches.

*3:Write the data into RAMs and read them out after the test interval.

*4:We assume only 3 cases are recorded out of 10-20 errors during the test, because the beam acceleration is too high for recording in hardware logs.

*5:Data marked with an error is written back once. But there is no effect on the program because the data is not used after the error occurs.

Neither program failure nor data integrity corruption even under 60M-130M times SER acceleration.

Summary

- SPARC64™ VI has achieved the following
  - High performance with 120W(max) power consumption:
    - Over 2X per socket performance of SPARC64V
  - High Reliability
    - All 1bit error in SRAM is correctable
    - Most of latches are parity protected, and 1bit error correctable through the unique instruction retry mechanism.

- Evolutionary development is a key to success.
  - SPARC64™ VI and the latest Mainframe CPU have been designed by the same experienced team.

- Improvements in SPARC64™ CPU's performance continue to increase the Fujitsu's UNIX® servers.

SPARC64™ VI